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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/053,963	01/22/2002	Aron T. Lunde	37829.0400	5214

7590 04/13/2006

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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 04/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/053,963	LUNDE, ARON T.	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 22nd, 2005 has been entered. A new rejection is made as set forth in this Office Action. Claims (1-28) are pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-20, 22-26, and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Chia et al. (U.S. Patent 5,923,047).

In re claim 1, **Chia** discloses a method for preparing a die on a wafer for testing by a testing apparatus, the method comprising, forming a die **12A-C** on a wafer **10**, the die **12A-C** having an active portion (top surface) comprising integrated circuitry, wherein the die **12A-12C** has a plurality of input bond pads **14** formed on the active portion (top surface); forming a plurality of test pads **20** on the die **12A-C**, the plurality of test pads **20** accessible to the testing apparatus, at least one of the plurality of test pads **12A-C**

corresponding to at least one of the plurality of input bond pads **14**; forming a conductive path (interconnects such as aluminum, col. 2, lines 40-44) between the at least one of the plurality of test pads **20** and the at least one of the plurality of input bond pads **14**, wherein a portion of the conductive path is formed on the die between an edge of the die **12A-C** and the active portion of the die **12A-C**; and testing the die **12A-C** by contacting the at least one of plurality of test pads **20** with the testing apparatus (col. 2, lines 10-58 and FIGS. 1-2).

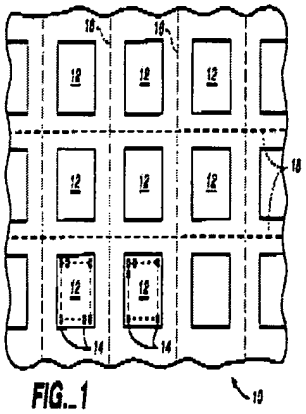

FIG._1

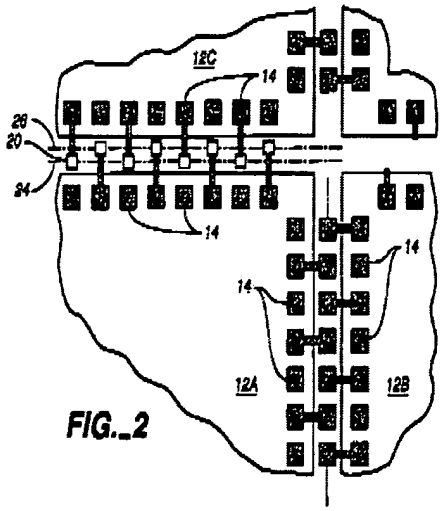

FIG._2

In re claims 2, 10, 15, and 23, **Chia** discloses wherein the plurality of test pads **14** is formed on the active portion (top surface) of the die **12A-C** (FIG. 2).

In re claims 3, 11, 16, and 24, **Chia** discloses the active portion (top surface of die **12A-C**) being surrounded by an inactive portion **24, 26**, wherein the conductive path extends from the at least one input bond pad **14** to the inactive portion and from the inactive portion to the at least one test pad **24** (col. 2, lines 10-58 and FIGS. 1-2).

In re claims 4, 17, and 25, **Chia** discloses portion of the conductive path is formed on wafer outside **26** of the die **12A-C** (FIG. 2).

In re claims 5 and 18, **Chia** discloses severing the conductive path at a point outside of the active portion (top surface) of the die **12A-C** (FIG. 2).

In re claims 6 and 19, **Chia** discloses severing the conductive path at a point within the inactive portion **24, 26** (FIG. 2)

In re claims 7 and 20, **Chia** discloses severing the conductive path at a point outside the die **12A-C** (FIG. 2).

In re claims 8 and 13, **Chia** discloses wherein at least one test pad **20** is of a sufficient size so as to be accessible by a testing apparatus (FIG. 2).

In re claim 9, **Chia** discloses a die assembly formed on a wafer, the die assembly comprising, a die **12A-C** formed on a wafer **10**, the die **12A-C** having an active portion (top surface) comprising integrated circuitry, wherein the die **12A-12C** has a plurality of input bond pads **14** formed on the active portion (top surface);

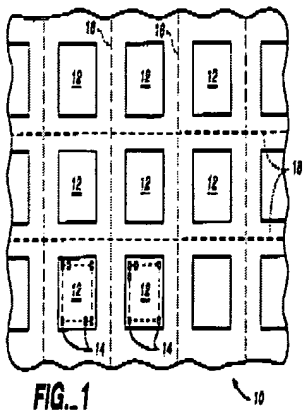

FIG._1

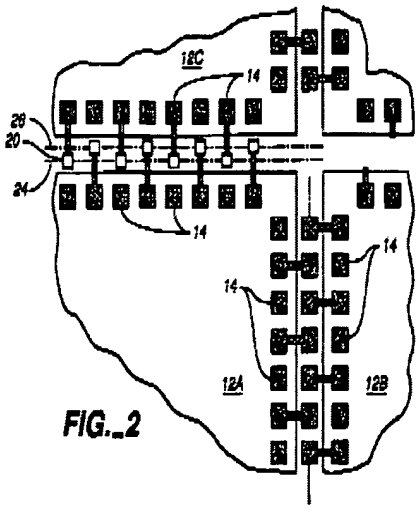

FIG._2

a plurality of test pads **20** on the die **12A-C**, the plurality of test pads **20** accessible to the testing apparatus, at least one of the plurality of test pads **12A-C** corresponding to at least one of the plurality of input bond pads **14**; a conductive path (interconnects such as aluminum, col. 2, lines 40-44) that electrically couples the at least one input bond pad **14** to the at least one test pad **20**, wherein a portion of the conductive path is formed on the die between an edge of the die **12A-C** and the active portion of the die **12A-C**; and testing the die **12A-C** by contacting the at least one of plurality of test pads **20** with the testing apparatus (col. 2, lines 10-58 and FIGS. 1-2).

In re claim 12, **Chia** discloses the die **12A-C** being surround by a non-conducting scribe area **24, 26** on the wafer **10**, wherein the portion of the conductive path is formed on the non-conducting scribe area **24, 26** (col. 2, lines 10-58 and FIG. 2).

In re claim 14, **Chia** discloses a method for preparing a die on a wafer for testing by a testing apparatus, the method comprising, forming a die **12A-C** on a wafer **10**, the die **12A-C** having an active portion (top surface) comprising integrated circuitry, wherein the die **12A-12C** has a plurality of input bond pads **14** formed on the active portion (top surface); forming a plurality of test pads **20** on the die 12A-C,

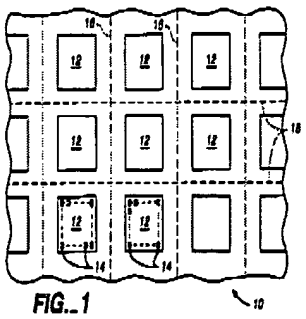

FIG._1

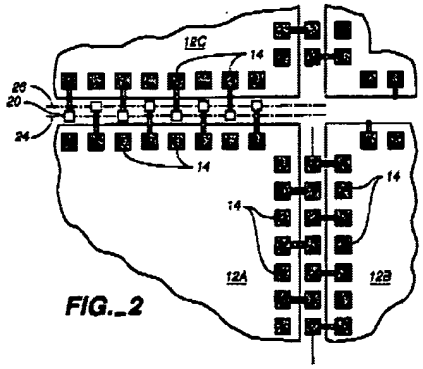

FIG._2

the plurality of test pads **20** accessible to the testing apparatus, at least one of the plurality of test pads **12A-C** corresponding to at least one of the plurality of input bond pads **14**; forming a conductive path (interconnects such as aluminum, col. 2, lines 40-44) between the at least one of the plurality of test pads **20** and the at least one of the plurality of input bond pads **14**, wherein a portion of the conductive path is formed on the die between an edge of the die **12A-C** and the active portion of the die **12A-C**; and testing the die **12A-C** by contacting the at least one of plurality of test pads **20** with the testing apparatus (col. 2, lines 10-58 and FIGS. 1-2).

In re claim 22, **Chia** discloses a die comprising, a die **12A-C** formed on a wafer **10**, the die **12A-C** having an active portion (top surface) comprising integrated circuitry, wherein the die **12A-12C** has a plurality of input bond pads **14** formed on the active portion (top surface); a plurality of test pads **20** on the die **12A-C**, the plurality of test pads **20** accessible to the testing apparatus, at least one of the plurality of test pads **12A-C** corresponding to at least one of the plurality of input bond pads **14**; a plurality of conductive lines (interconnects such as aluminum, col. 2, lines 40-44),

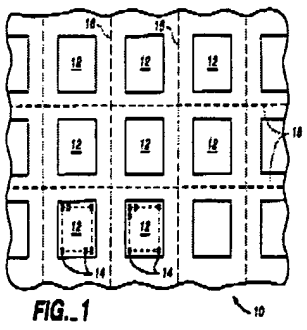

FIG._1

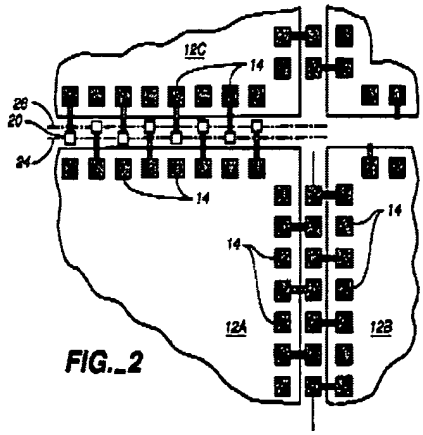

FIG._2

wherein each of the conductive lines is initially formed to electrically couple at least one of plurality of input bond pad **14** to at least one of the plurality of test pad **20**, and wherein a portion of the conductive lines is formed on an area between an edge of the die **12A-C** and the active portion of the die **12A-C**; and testing the die **12A-C** by contacting the at least one of plurality of test pads **20** with the testing apparatus (col. 2, lines 10-58 and FIGS. 1-2).

In re claim 26, **Chia** discloses wherein portion of each of the conductive lines is severed when the die **12A-C** is separated from the wafer **10** (FIGS. 1-2).

In re claim 28, **Chia** discloses a die comprising, an active portion (top surface) comprising integrated circuitry **12A-C**, a plurality of input bond pads **14** formed on the active portion (top surface); a plurality of test pads **20** formed on the die **12A-C**, a conductive lines (interconnects such as aluminum, col. 2, lines 40-44), wherein each of the conductive lines is initially formed to electrically couple the at least one of the plurality of input bond pad **14** to the at least one of the plurality of test pad **20**, and wherein a portion of each of the conductive lines is formed on a scribe area **24, 26** outside the die **12A-C** (col. 2, lines 10-58 and FIGS. 1-2).

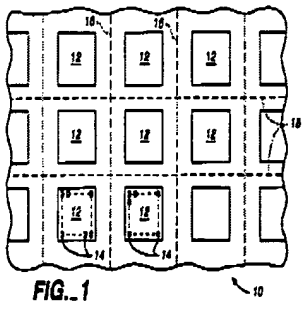

FIG._1

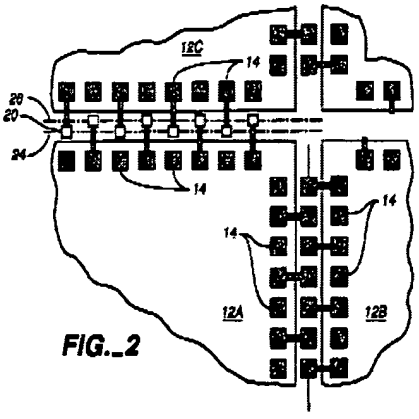

FIG._2

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 21 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chia et al. (U.S. Patent 5,923,047).

In re claims 21 and 27, Chia does not explicitly disclose that the at least one of the plurality of test pads **20** is larger in size than the at least one of the plurality of input bond pads **14**. However, there is no evidence indicating the size and shape of the plurality of test pads and input bond pads is critical and it has been held that it is not inventive to discover the optimum or workable size or shape of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Response to Applicant's Amendment and Argument

Applicant contend that the reference Hubacher (U.S. Patent 5,554,940) herein known as Hubacher teaches a die wherein a test pad interconnect (reference **36**) contacts

a via pad (reference number **34**) and a test pad (reference number **28**) in an area not between an edge of die **10** and an active portion of die **10** (i.e., bond pad 12).

In response to applicant's contention that Hubacher does not teach or suggest each of the elements of claim 1 (i.e., said conductive path is formed on said die between an edge of said die and said active portion of said die) as recited in the (currently amended) independent claims, Examiner respectfully submits that Applicant's argument is moot in view of the newly discovered reference to Chia et al. (U.S. Patent 5,923,047). Applicant is directed to (col. 2, lines 10-58 and FIGS. 1-2) where Chia disclose wherein a portion of the conductive path is formed on the die **12A-C** between an edge of the die **12A-C** and the active portion (top surface) of the die **12A-C** and testing the die by contacting the at least one of plurality of test pads **20** with the testing apparatus (col. 2, lines 10-58 and FIGS. 1-2).

For this reason, Examiner holds the rejection proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
April 10, 2006

W. DAVID COLEMAN
PRIMARY EXAMINER